

FSROH_D CORE CELL

0.11 μm HIGH PERFORMANCE HIGH DENSITY STANDARD CELLS

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Key Features

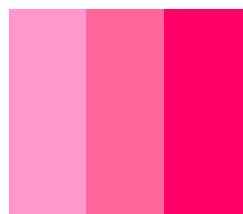
- UMC's 0.11 μm 1P8M FSG logic process
- Raw gate density: 300k gates/ mm^2 offers high density needed for low cost applications
- A wide range of drive strengths and optimized P/N ratio for superior performance
- A complete set of models for industry-standard EDA tools
- A full set of gated clock buffers for power saving
- Each cell has at least one sub/well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR drop in filler cells
- 1.2 V \pm 10 % characterization range
- Optional 1.0 V \pm 10 % characterization range

General Description

This library is tailored for UMC's 0.11 μm 1P8M FSG logic process. It is especially suitable for high performance/high density applications. Along with a wide selection of drive strengths, the 8-track (2.88 μm) cell height enables users to implement high performance designs with the smallest area. To maximize yield, Faraday ensures all cells have no bent gate transistors. This library can be customized to provide new cells for customers by following Faraday's internal evaluation procedures.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.11 μm 1P8M FSG logic process
	Drawn gate length	0.12 μm
	Gate density	300k gates/ mm^2
	Core cell height	2.88 μm (8-track)
	Vertical/Horizontal routing grid	0.36 μm
	Power/Ground rail width	0.504 μm
	Layout resolution	0.009 μm
Electrical	Recommended operating conditions	Supply voltage: 1.2 V Junction temperature: -40 $^{\circ}\text{C}$ ~ 125 $^{\circ}\text{C}$
	Speed	Td = 25.4 ps/stage (Measured from 101-stage NAND2 ring for typical process at 1.2 V and 25 $^{\circ}\text{C}$)
	Power consumption	7.2 nW/MHz/gate (Measured from NAND2 chain, output load = 2 inverters in typical process and operated under 1.2 V and 25 $^{\circ}\text{C}$)
	Drive strengths level	Up to 12 (depending on respective cells)



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