

# SYNCHRONOUS HIGH DENSITY SINGLE-PORT SRAM COMPILER

Version 1.0 | August 2006

## Key Features

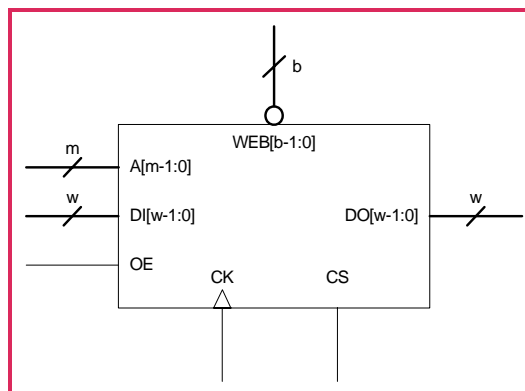
- Synchronous read and write operations
- Full customized layout density per customers' configurations
- High density, available in  $1.2\text{ V} \pm 10\%$
- Automatic power down to eliminate the DC current
- Clocked address inputs and CS to the RAM at the CK rising edge
- Clocked web input pins to the RAM at the CK rising edge
- Clocked DI input pins to the RAM at the CK rising edge
- Byte/Word write operations available
- Verilog/VHDL timing/simulation model generators
- SPICE netlist generator
- GDSII layout generator
- Memaker preview UI
- Supports the BIST codes
- Multi-block options for the best aspect ratio

## General Description

FSR0H\_D\_SH is a synchronous, high-density single-port SRAM compiler. This SRAM compiler is implemented using UMC 0.11  $\mu\text{m}$  logic HS (FSG) process design rules and can be incorporated with Faraday's 0.11  $\mu\text{m}$  standard cells. This product allows different combinations of words, bits, and aspect ratios to be used for generating the most desirable configurations.

Given the desired size and timing constraints, the FSR0H\_D\_SH compiler is capable of providing suitable synchronous RAM layout instances in seconds. It can automatically generate the data sheets, Verilog/VHDL behavioral simulation models, SCS or ViewLogic symbols, place and route models, and the test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are satisfied. This provides a more flexible CK falling edge during each operation. Both the word/byte write operations and the simulation models are available.

## Logic Symbol



# FSROH\_D\_SH

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### Quick Reference

Bit cell	UMC.L110E 6TSRAM1.85HSSP
Cycle time	348 MHz (max.) under the worse case condition of 4K x 16
Address port	One read/write port
Variable capacity	1M bits (max.)
Output buffer	Tri-state
Aspect ratio (multi-block options)	1, 2, 4, 8, 16
Application	Configurable SRAM modules for the embedded designs on UMC 0.11 $\mu\text{m}$ logic HS (FSG) process



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