

# SYNCHRONOUS HIGH SPEED ONE-PORT REGISTER FILE COMPILER

Version 1.0 | August 2006

## Key Features

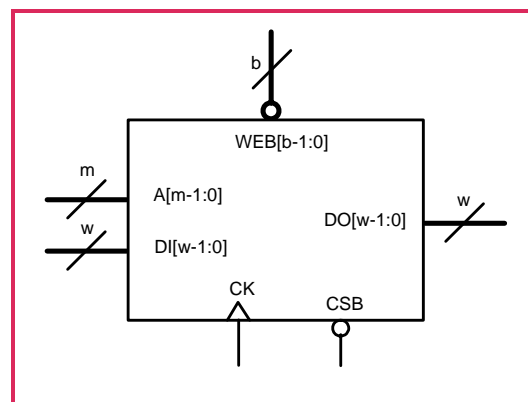
- Synchronous read and write operations
- Fully customized layout density
- 1.2 V  $\pm$  10% operating voltage available
- Automatic power down to eliminate the DC current
- Clocked address inputs and CSB to the RAM at the CK rising edge
- Clocked weband DI input pins to the RAM at the CK rising edge
- Byte write and word write operations available
- Verilog/VHDL timing/simulation model generators
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST codes
- Column Mux options for the best aspect ratio

## General Description

FSROH\_D\_SY is a synchronous, one-port register file compiler. It was created according to UMC's 0.11  $\mu\text{m}$  logic HS (FSG) process design rules and can be incorporated with Faraday's 0.11  $\mu\text{m}$  standard cells. Selectable combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSROH\_D\_SY compiler is capable of providing suitable synchronous RAM layout instances in minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, SCS or ViewLogic symbols, place & route models, and the test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are satisfied. This allows a more flexible clock falling edge in each operation. Both word/byte write operations and simulation models are available.

## Symbol Diagram



# FSROH\_D\_SY

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#### Quick Reference

Bit cell	UMC L110E 6TSRAM1.85HSSP
Cycle time	340 MHz (max.) under the worst case condition of 1K x 16
Address port	Single read/write port
Variable capacity	72 kB (max.)
Aspect ratio (Column Mux)	2, 4, 8
Application	Configurable SRAM modules of the embedded design using 0.11 $\mu$ m logic HS (FSG) process





#### **HEADQUARTERS**

Hsinchu, Taiwan,  
Tel: 886-3-578-7888  
Fax: 886-3-578-7889  
twsales@faraday-tech.com

#### **USA OFFICE**

Sunnyvale, USA  
Tel: 1-408-522-8888  
Fax: 1-408-522-8889  
ussales@faraday-tech.com

#### **EUROPE OFFICE**

Hoofddorp, Netherlands  
Tel: 31-2356-20496  
Fax: 31-2356-36297  
eusales@faraday-tech.com

#### **JAPAN OFFICE**

Tokyo, Japan  
Tel: 81-3-5214-0070  
Fax: 81-3-5214-0076  
jpsales@faraday-tech.com

#### **CHINA OFFICE**

Shanghai, P. R. China  
Tel: 86-21-6406-7523  
Fax: 86-21-6406-5327  
cnsales@faraday-tech.com