

# 0.13μm Synchronous High Density Single Port SRAM Compiler – FSC0H\_D\_SH

## Key Features

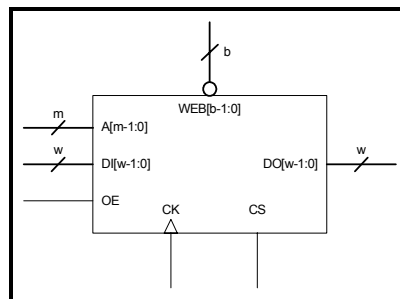
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range: -40° ~ 125°C
- Recommended operating ambient temp. range: 0° C ~ 85° C
- Minimum metal requirement: 5 metal layers
- Synchronous read and write operations
- Full custom layout density per customer configuration
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to RAM with CK rising edge
- Clocked WEB input pin to RAM with CK rising edge
- Clocked DI input pins to RAM with CK rising edge
- Byte write or word write operations available
- Verilog / VHDL timing / simulation model generator
- SPICE netlist generator
- GDSII layout generator
- Memory compiler preview UI (memaker)
- BIST code supported
- Multi-block options for the best aspect ratio

## General Description

The FSC0H\_D\_SH is a synchronous high density, single port SRAM. It is implemented using UMC's 0.13μm 1P8M 1.2V standard logic HS CMOS process design rules and can be incorporated with Faraday's 0.13μm standard cells. This product allows different combinations of words, bits, and aspect ratios to be used for generating the most desirable configurations.

By requesting the desired size and timing constraints, the FSC0H\_D\_SH compiler is capable of providing suitable synchronous RAM layout instances in seconds. It can automatically generate data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This provides the flexibility of CK falling edge during each operation. Both word write and byte write operations are supported.

## Symbol



## Quick Reference

Maximum Capacity	1M bits
Maximum Words	128K
Minimum Words	96
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8, 16

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