

# FSC0H\_D\_SP

## 0.13 $\mu\text{m}$ SYNCHRONOUS HIGH-SPEED VIA1 PROGRAMMABLE ROM COMPILER

Version 1.2 | September 2006

### Key Features

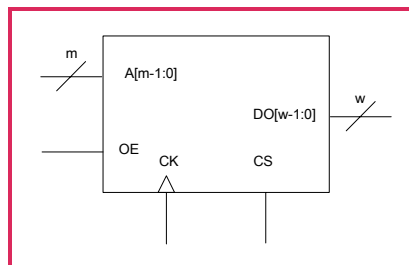
- Synchronous read operation
- Fully customized layout density
- High density available in  $1.2\text{ V} \pm 10\%$
- Automatic power down to eliminate the DC current
- Minimum metal requirement: 5 metal layers
- Clocked address inputs and CS to ROM at the CK rising edge
- Programmable Via1 layer code
- Verilog/VHDL timing simulation model generators
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports BIST code
- Multi-block options for the best aspect ratio

### General Description

The FSC0H\_D\_SP is a synchronous high-speed Via1 programmable ROM compiler. It was created according to UMC 0.13  $\mu\text{m}$  logic EHS (FSG) process design rules and can be incorporated with Faraday 0.13  $\mu\text{m}$  standard cells. Selectable combinations of words, bits, and aspect ratios can be used to generate the most desirable configuration.

Given the desired size and timing constraints, the FSC0H\_D\_SP compiler is capable of providing the suitable synchronous ROM layout instances in minutes. It automatically generates the data sheet, Verilog/VHDL behavioral simulation model, SCS or ViewLogic symbol, Place & Route models and the test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are satisfied. This allows a more flexible clock falling edge in each operation.

### Symbol Diagram



### Quick Reference

Cycle time	319 MHz (max.) under the worst case condition of 4K x 16
Address port	1 read port
Variable capacity	2 MB (max.)
Output buffer	Tri-state
Aspect ratio (Multi-block option)	1, 2, 4, 8
Application	Compliable ROM modules of the embedded design using UMC 0.13 $\mu\text{m}$ logic EHS (FSG) process



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