

0.13μm Synchronous High Speed 2- Port Register File Compiler – FSC0H_D_SW

Key Features

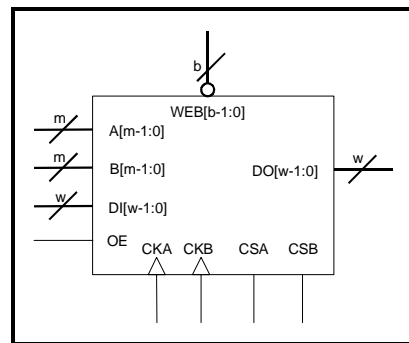
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 5 metal layers
- Synchronous read and write operations
- Fully customized layout density per customer configuration
- Automatic power down to eliminate DC current
- Clocked address inputs and CSA (B) to RAM with CKA (B) rising edge
- Clocked WEB input pin to RAM with CKB rising edge
- Clocked DI input pins to RAM with CKB rising edge
- Byte write or word write operations available
- Memory compiler preview UI (Memaker)
- BIST circuit supported
- Column Mux options for the best aspect ratio

General Description

The FSC0H_D_SW is a synchronous, high speed, 2-port register file. It is implemented according to UMC's 0.13μm high speed technology. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSC0H_D_SW compiler is capable of providing suitable synchronous RAM layout instances in minutes. It also automatically generates data sheets, Verilog behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in the ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This allows the flexibility of clock falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

Maximum Capacity	72K bits
Maximum Words	4K
Minimum Words	16
Maximum Bits	144
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux)	2, 4, 8, 16

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