

0.13μm Synchronous High Speed Single Port Register File Compiler – FSC0H_D_SY

Key Features

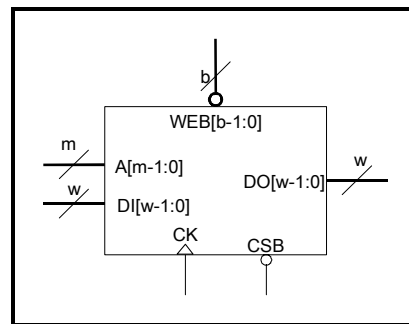
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 5 metal layers
- Synchronous read and write operations
- Fully customized layout density
- Automatic power down to eliminate DC current
- Clocked address inputs and CSB to RAM at CK rising edge
- Clocked WEB input pin to RAM at CK rising edge
- Clocked DI input pins to RAM at CK rising edge
- Byte write or word write operations available
- Memory compiler preview UI (Memaker)
- BIST circuitry supported
- Column mux options for the best aspect ratio

General Description

The FSC0H_D_SY is a synchronous, high speed, single port register file. It is implemented according to UMC's 0.13μm high speed technology. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSC0H_D_SY compiler is capable of providing suitable synchronous RAM layout instances in minutes. It also automatically generates data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This allows the flexibility of a clock falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

| | |
|---------------------------|----------|
| Maximum Capacity | 72K bits |
| Maximum Words | 2K |
| Minimum Words | 32 |
| Maximum Bits | 144 |
| Minimum Bits | 1 |
| Bit Increment | 1 |
| Aspect Ratio (Column Mux) | 2, 4, 8 |

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