

0.13μm High Performance FSC0H_D SSTL2 (ClassII) / LVTTTL (20mA) Combo I/Os

Key Features

- UMC's 0.13μm 1.2V/3.3V HS/FSG/L130E Logic Process
- 3.3V LVTTTL input, 3.3V LVTTTL output drive
- 2.5V SSTL2 input, 2.5V SSTL2 output drive
- Output buffer with SSTL2 (ClassII) / LVTTTL (20mA) driving strength
- Input buffer with Schmitt trigger in LVTTTL mode, power down function in SSTL2 mode
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

Faraday's SSTL-2 with ClassII driving strength & LVTTTL with 10mA driving strength Combo I/O cells are designed to meet JEDEC standard JESD8-9B (for SSTL-2) and JESD8-B (for LVTTTL). All SSTL-2 & LVTTTL Combo I/O cells are designed according to UMC's 0.13μm 1.2V/3.3V high speed enhancement Logic Process.

In order to handshake with modern DDR SDRAM memory subsystem, all members in this family are designed to operate up to DDR-400 upon specified termination. By using these cells with suitable configurations, the signal convention can also be processed to provide compatibility with LVTTTL relative subsystem.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.13μm 1.2V/3.3V 1P8M HS Logic Process
	Cell Width * Cell Height	68μm * 218.4μm (Single ended bi-direction buffer)
		109.6μm * 218.4μm (Differential output buffer)
		34.8μm * 218.4μm (Single ended input buffer)
		69.6μm * 218.4μm (Differential input buffer)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M4 and above
Layout resolution	0.01μm	
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.08V ~ 1.32V I/O: 2.3V ~ 2.7V (SSTL2) I/O: 2.97V ~ 3.63V (LVTTTL)
		Junction Temperature: -40°C ~ 125°C
	Driving Strength	Class II (SSTL2)/ 20mA (LVTTTL)
	Input Threshold	SSTL2/LVTTTL

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