

## 0.13μm 1.2V/3.3V HS/FSG Logic Process

### FSC0H\_D 3.3V Analog ESD Protection Set

#### Key Features

- UMC's 0.13μm 1.2V/3.3V HS/FSG/L130E Logic Process
- 3.3V ESD protection cells for analog I/O
- 3.3V Power / Ground cells with ESD protection
- Power-cut cells with ESD protection to separate 3.3V analog blocks from digital
- ESD robustness and Latch-up immunity proven by silicon

#### General Description

This I/O set is tailored for UMC's 0.13μm 1.2V/3.3V HS/FSG/L130E Logic Process. This set provides a full ESD protection for an isolated analog block. Two layout structures, both optimized for pad limited and core limited designs, are available.

#### Quick Reference

Characteristic		Description
<b>Physical</b>	Process	UMC 0.13μm 1.2V/3.3V 1P8M HS/FSG Logic Process
	Cell Height	218.4μm (Staggered) 152.0μm (In-line)
	Cell Width	Multiples of 0.4μm
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M4 and above
	Layout Resolution	0.01μm
<b>Electrical</b>	Recommended Operating Conditions	Power supply voltage Core: 1.08V to 1.32V I/O: 2.97V~3.63V
		Junction temperature: -40°C ~ 125°C

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