

0.13μm High Performance PECL IOs

FSC0H_D PECL I/O Cells

Key Features

- UMC's 0.13μm 1.2V/3.3V HS/FSG/L130E Logic Process
- 3.3V PECL I/O cells
- Options for 25 ohms and 50 ohms output buffers
- 300MHz for differential type drivers and receivers
- 250MHz for single-ended type driver and receivers
- Support power down mode
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

This library is tailored for UMC's 0.13μm 1.2V/3.3V HS/FSG/L130E Logic Process. For high-speed chip-to-chip communications with specified DC drive characteristics, these differential type receivers and drivers provide data transfer rates up to 300Mbps. Single-ended type buffers are provided for lower power consumption. For improved noise performance (due to common mode noise rejection) these cells provide differential type buffers. Staggered and In-line structures are provided for all PECL I/O cells to fit pad limit or core limit designs.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.13μm 1.2V/3.3V 1P8M HS Logic Process
	Cell Width * Cell Height	34.8μm * 218.4μm (Staggered single ended input buffer)
		36.0μm * 218.4μm (Staggered single ended output buffer)
		60.0μm * 152.0μm (In-line single ended input buffer)
		60.8μm * 152.0μm (In-line single ended output buffer)
	Cell Layout Metal	M1, M2, M3
Power Ring Metal	M4 and above	
Layout resolution	0.01μm	
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.08V ~ 1.32V I/O: 2.97V ~ 3.63V
		Junction Temperature: -40°C ~ 125°C
	Output impedance	25 Ohms and 50 Ohms

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