

Delay Locked Loop FXDLL311HC0H

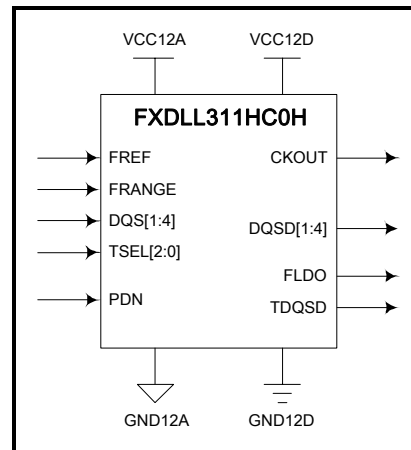
Key Features

- UMC 0.13 μ m 1.2V 1P8M HS process
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temperature range: -40°C ~ 125°C
- Recommended operating ambient temperature range: 0°C ~ 85°C
- IP's minimum metal requirement: 4 metal layers
- Pure 1.2V power supply
- DDR SDRAM controller usage
- Four channels with 20% DQS delay
- Low jitter output
- Power-down mode
- No external component required

General Description

FXDLL311HC0H is a 0.13 μ m Delayed-Locked Loop (DLL) IP that generates four-channel DQS with fixed timing delay and four-channel test mode for DDR SDRAM controller usage. It can also process input clock frequencies ranging from 100MHz to 200MHz (DDR-200 / 266 / 333 / 400). This DLL can be used in DDR SDRAM controller to generate 20% delay in period of FREF for DQS signal to do DQ data latch process.

Symbol



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