

Phase-Locked Loop

FXPLL110HC0H_APGD

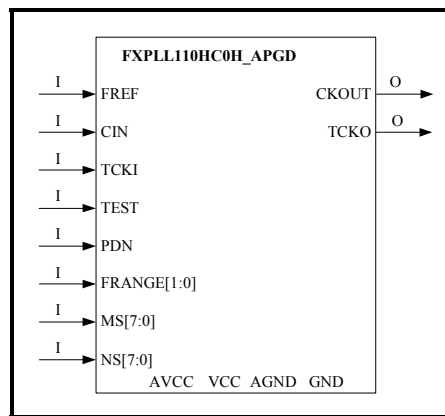
Key Features

- UMC 0.13 μ m 1.2V High Speed 1P8M Logic process
- Operating voltage range: 1.08V ~ 1.32V
- IP's minimum metal requirement: 4 metal layers
- Included power/ground I/O cells.
- Low jitter output
- Power-down mode
- No external component required

General Description

The FXPLL110HC0H_APGD is a 0.13 μ m Phase-Locked Loop (PLL) IP that multiplies slower input signal and/or de-skew clock. It can generate wide range clock from 62.5MHz to 1GHz ; and the output clock is a stable, low-jitter signal. This IP can be used in consumable electric product or CPU.

Symbol



Quick Reference (Implementation Section)

Pin Name	I/O Type	Function Description
FREF	Input	Reference input clock (5MHz ~100MHz).
CKOUT	Output	Output clock (62.5MHz ~ 1000MHz).
CIN	Input	Feedback clock.
MS[7:0]	Input	Programmable pre-divider, 8 bits (1 ~ 255).
NS[7:0]	Input	Programmable loop divider, 8 bits (1 ~ 255).
PDN	Input	Power-down mode setting, active Low.
FRANGE[1:0]	Input	Control pins to select frequency range of CKOUT.
TEST	Input	Test mode setting, active High.
TCKI	Input	Testing clock input, used in test mode.
TCKO	Output	Testing clock output (CKOUT/32), used in test mode.
AVCC	Power pad	Analog power, typical case, 1.2V.
AGND	Ground pad	Analog ground.
VCC	Power pad	Digital power, typical case, 1.2V.
GND	Ground pad	Digital ground.

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