



0.13μm Low Leakage 3.3V with 5V Tolerance Generic I/Os FSC0L_D 3.3V with 5V Tolerance Generic I/O Cells

Key Features

- UMC's 0.13μm 1.2V/3.3V LL/FSG/L130E Logic Process
- 3.3V with 5V tolerance input, 3.3V output drive
- Output buffer with programmable drive strength from 2mA to 8mA with 2mA step, 4mA to 16mA with 4mA step
- Input buffer with programmable pull up resistance, pull down resistance, keeper, and Schmitt trigger
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

This library is tailored for UMC's 0.13μm 1.2V/3.3V LL/FSG/L130E Logic Process. All I/Os are equipped with a rich selection of programmable features capable of adapting to a wide variety of application environments. Two layout structures, both optimized for pad limited and core limited designs, are available to support each programmable feature or function.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.13μm 1.2V/3.3V 1P8M LL/FSG/L130E Logic Process
	Cell Width * Cell Height	44.0μm * 218.4μm (Staggered) 79.2μm * 152.0μm (In-line)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M4 and above
	Layout resolution	0.01μm
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.08V to 1.32V I/O: 2.97V~3.63V
		Junction Temperature: -40°C ~ 125°C
	Driving Strength	2mA~8mA by 2mA step, 4mA~16mA by 4mA step
	Input Threshold	LVTTL
	Pull Up/Down resistance	75K Ohm

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