

0.13μm Synchronous Low Leakage High Density Single Port Static Memory Compiler – FSC0L_D_SH

Key Features

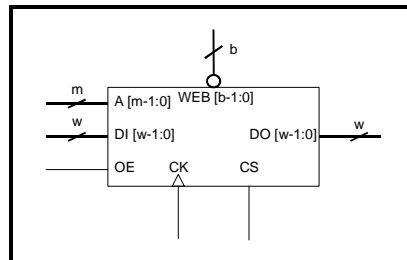
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 5 metal layers
- Synchronous read and write operations
- Fully customized layout density per customer configuration
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to RAM with CK rising edge
- Clocked WEB input pin to RAM with CK rising edge
- Clocked DI input pins to RAM with CK rising edge
- Byte write or word write operations available
- Memory compiler preview UI (memaker)
- BIST circuitry supported
- Multi-block options for the best aspect ratio

General Description

The FSC0L_D_SH is a synchronous low leakage, high density single port SRAM. It is implemented according to UMC's 0.13μm fusion technology. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSC0L_D_SH compiler is capable of providing suitable synchronous SRAM layout instances in minutes. It also automatically generates data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This provides the flexibility of clock falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

Maximum Capacity	1M bits
Maximum Words	128K
Minimum Words	96
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8, 16

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