

0.13μm Synchronous Low Leakage Dual-Port Static Memory Compiler – FSC0L_D_SJ

Key Features

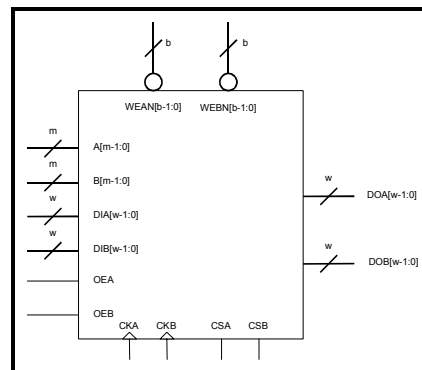
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 6 metal layers
- Synchronous read and write operations
- Fully customized layout density
- Automatic power down mechanism to eliminate DC current
- Clocked address inputs and CSA(B) to RAM with CKA(B) rising edge
- Clocked WEA(B)N input pins to RAM with CKA(B) rising edge
- Clocked DIA(B) input pins to RAM with CKA(B) rising edge
- Byte write or word write operations available
- Memory compiler preview GUI (Memaker)
- BIST code supported
- Column MUX options for the best aspect ratio

General Description

The FSC0L_D_SJ is a synchronous, low leakage, dual-port SRAM. It is created according to UMC's 0.13μm LL/FSG technology. Different combination of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSC0L_D_SJ compiler is capable of providing suitable synchronous SRAM layout instances in minutes. It also automatically generates data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The length of duty cycle can be neglected as long as the setup / hold time and minimum widths of high / low pulse are satisfied. This allows the flexibility of a clock falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

Maximum Capacity	512K bits
Maximum Words	8K
Minimum Words	32
Maximum Bits	256
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux options)	4, 8, 16

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