

Key Features

- UMC's 0.13μm 1.2V/3.3V LL/FSG/L130E Logic Process
- High frequency oscillator pad range: 1MHz ~ 66MHz
- Low frequency oscillator pad range: 32KHz ~ 1MHz
- Programmable output driving capability
- Oscillation mode / power down (stop) mode / tri-state mode / parallel model
- Internal feedback resistance
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

This library is tailored for UMC's 0.13μm 1.2V/3.3V LL/FSG/L130E Logic Process. All I/O cells have been designed as programmable crystal oscillator I/O cells. Two layout structures, both optimized for pad limited and core limited designs, are available to support each programmable feature or function.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.13μm 1.2V/3.3V LL/FSG/L130E Logic Process
	Cell Width * Cell Height	69.6μm * 218.4μm (Staggered) 120.0μm * 152.0μm (In-line)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M4 and above
	Layout resolution	0.01μm
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.08V ~ 1.32V I/O: 2.97V ~ 3.63V Junction Temperature: -40°C ~ 125°C
	Frequency	High frequency oscillator pad :1M ~ 66M Low frequency oscillator pad :32K ~ 1M
	Input Threshold	LVTTL

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