



0.13μm Standard Performance High Density Generic Core Cells - FSC0G_D Core Cell

Key Features

- UMC's 0.13μm 1.2V/3.3V SP/FSG/L130E Logic Process
- Raw gate density: 250,000 gates/mm² offers high density needed for low cost applications
- Wide drive strength range and optimized P/N ratio for performance
- Complete set of models for industry-standard EDA tools
- Full set of gated clock buffers for power saving
- Only Metal 1 used in layout, each cell has at least one sub / well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR-drop in filler cells

General Description

This library is tailored for UMC's "0.13μm 1.2V/3.3V Logic Standard Performance Process". It is especially suitable for high speed / high density applications. The 8-track (3.2μm) cell height along with a wide selection of drive strengths enable customers to implement high performance designs with smallest area. To maximize yield, Faraday ensures all cells have no bent-gate transistors. This library can be customized to provide new cells for customers, following Faraday's internal evaluation procedures.

Quick Reference

Characteristic		Description
Physical	Process	UMC's 0.13μm 1.2V / 3.3V 1P8M SP Logic Process
	Drawn Gate Length	0.12μm
	Gate Density	250,000 gates/mm ²
	Core Cell Height	3.2μm (8-track)
	Vertical / Horizontal Routing Grid	0.40μm / 0.40μm
	Power / ground rail width	0.56μm
	Layout resolution	0.01μm
Electrical	Recommended Operating Conditions	Power Supply Voltage: 1.08V to 1.32V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 28.8ps/stage (Measured from 101-stage NAND2 ring for typical process at 1.2V and 25°C)
	Power Consumption	6nW / MHz / gate (Measured from NAND2 chain, output load = 2 INVERTER in typical process and operated under 1.2V, 25°C)
	Drive Strengths Level	Up to 12 (Depending on cell)

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