FSL0A_C

0.153 µm GENERIC CORE CELL LIBRARY

Version 1.0 | December 2008

Key Features

- UMC 0.153 µm logic process
- Raw gate density: 110,000 gates/mm^2 target for the low-cost applications
- A wide range of drive strengths and optimized P/N ratios for superior performance
- Supports a complete set of models for the industry-standard EDA tools
- Supports a full set of gated clock buffers for saving power
- Only M1 layer is used for layout
- Supports the flexible row abutment

General Description

FSL0A_C is tailored for the UMC 0.153 µm logic process. It is especially suitable for the high-speed/high-density applications. The 9-track (5.04 µm) cell height along with a wide range of drive strengths enables customers to implement the high performance designs with the smallest area. This library can be customized to provide new cells, following Faraday internal evaluation procedures.

Quick Reference

Physical	Process	UMC 0.153 µm logic process
	Drawn gate length	0.18 µm
	Gate density	110,000 gates/mm^2
	Core cell height	5.04 µm (9-track)
	Vertical/Horizontal routing grid	0.56 µm/0.62 µm
	Power/Ground rail width	0.76 µm
	Layout resolution	0.01 µm
Electrical	Recommended operating condition	Power supply voltage range: 1.62 V ~ 1.98 V
		Operating junction temperature range: -40 °C ~ 125 °C
	Speed	T_d = 39.6 ps/stage (Measured from the 101-stage NAND2 ring in the typical process, operating at 1.8 V and 25 °C)
	Power consumption	23 nW/MHz/gate (Measured from the NAND2 chain, output load = 2 inverters in the typical process, operating at 1.8 V and 25 °C)
	Drive strengths level	Up to 8, depending on the cell type

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