FSL0A_C_SJ

SYNCHRONOUS HIGH-DENSITY DUAL-PORT SRAM COMPILER

Version 1.0 | October 2008

Key Features

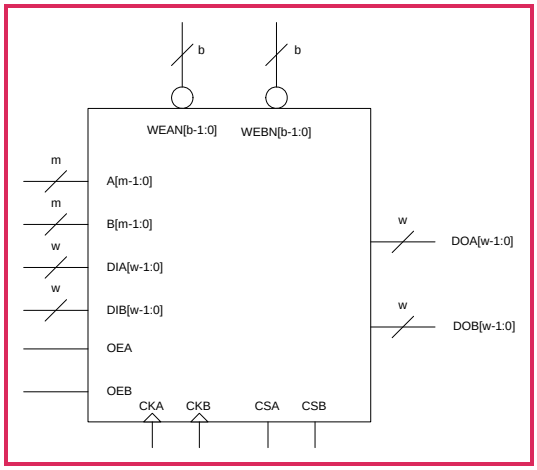
- Synchronous read and write operations
- Fully-customized layout density available at 1.8 V ± 10%
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CSA(B) to the RAM at the CKA(B) rising edge
- Clocked WEA(B)N input pins to the RAM at the CKA(B) rising edge
- Clocked DIA(B) input pins to the RAM at the CKA(B) rising edge
- Supports byte write and word write operations
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST code
- Column Mux options for the best aspect ratio
- Minimum metal requirement: 5 metal layers

General Description

FSL0A_C_SJ is a synchronous high-density and dual-port SRAM compiler. It was implemented according to the UMC 0.153 μm logic process design rules and can be incorporated with the Faraday 0.153 μm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configuration.

Given the desired size and timing constraints, the FSL0A_C_SJ compiler is capable of providing suitable synchronous RAM layout instances within minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, Place & Route models, and test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are both satisfied. This allows a more flexible clock falling edge in each operation. Both word write and byte write operations are supported.

Logic Symbol



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