

## SYNCHRONOUS TWO-PORT REGISTER FILE COMPILER

Version 1.0 | November 2008

### Key Features

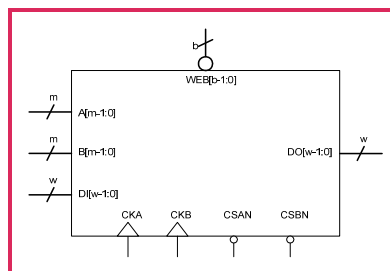
- Operating voltage range: 1.62 V ~ 1.98 V
- Operating junction temperature range: -40 °C ~ 125 °C
- Minimum metal requirement: 4 metal layers
- Synchronous read and write operations
- Fully-customized layout density
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CSA(B)N to RAM with the CKA(B) rising edge
- Clocked WEB input pins to RAM with the CKB rising edge
- Clocked DI input pins to RAM with the CKB rising edge
- Byte write or word write operations available
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST code
- Column Mux options for the best aspect ratio

### General Description

FSLOA\_C\_SZ is a synchronous, two-port register file compiler. It is implemented according to the UMC 0.153  $\mu\text{m}$  logic process design rules and can be incorporated with Faraday 0.153  $\mu\text{m}$  standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

Given the desired size and timing constraints, the FSLOA\_C\_SZ compiler is capable of providing suitable synchronous RAM layout instances within minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, Place & Route models, and test patterns used in ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold time and minimum high/low pulse widths are satisfied. This provides a more flexible CK falling edge during each operation. Both word write and byte write operations are supported.

### Logic Symbol



### Quick Reference

Maximum capacity	72k bits
Maximum words	2k
Minimum words	8
Maximum bits	144
Minimum bits	1
Bit increment	1
Aspect ratio (Column Mux options)	2, 4, 8

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