

# SYNCHRONOUS HIGH-DENSITY LOW POWER SINGLE-PORT SRAM COMPILER

Version 1.0 | October 2008

## Key Features

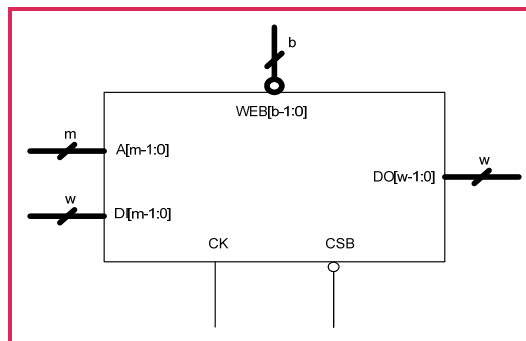
- Synchronous read and write operations
- High-density, low power, and a small memory design area
- Fully-customized layout density
- Available at  $1.8\text{ V} \pm 10\%$  and  $1.5\text{ V} \pm 10\%$
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CSB to RAM at the CK rising edge
- Clocked DI/WEB input pins to RAM at the CK rising edge
- Both byte write and word write operations available
- Verilog/VHDL timing/simulation model generators
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST code
- Column Mux options for the best aspect ratio
- Minimum metal requirement: 5 metal layers

## General Description

FSLOA\_D\_SL is a high-density, low power, synchronous single-port SRAM compiler with a smaller area. It was created according to the UMC 0.153  $\mu\text{m}$  logic process design rules and can be incorporated with Faraday 0.153  $\mu\text{m}$  standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

Given the desired size and timing constraints, the FSLOA\_D\_SL compiler is capable of providing suitable synchronous RAM layout instances within minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, Place & Route models, and test patterns to be used in the ASIC designs. The length of duty cycle can be neglected as long as the setup/hold time and the minimum high/low pulse widths are satisfied. This allows a more flexible clock falling edge in each operation. Both word/byte write operations and simulation models are available.

## Symbol Diagram



# FSLOA\_D\_SL

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### Quick Reference

Cycle time	250 MHz (Max.) under the worse case condition of 2K x 32 (1.62 V)
Address port	Single read/write port
Variable capacity	512 KB (Max.)
Output buffer	Tri-state
Aspect ratio (Column Mux)	16, 32, 64
Application	Configurable SRAM modules of the embedded designs by using the UMC 0.153 $\mu$ m logic process

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