

SYNCHRONOUS VIA1 PROGRAMMABLE ROM COMPILER

Version 1.0 | October 2008

Key Features

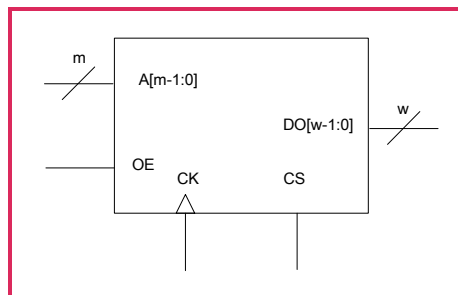
- Synchronous read operation
- Fully-customized layout density available at $1.8\text{ V} \pm 10\%$
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CS to ROM at the CK rising edge
- Minimum metal requirement: 5 metal layers
- Programmable Via1 layer codes
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST code
- Multi-block options for the best aspect ratio

General Description

FSLOA_D_SP is a synchronous Via1 programmable ROM compiler. It was created according to the UMC 0.153 μm logic process design rules and can be incorporated with Faraday 0.153 μm standard cells. Selectable combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

Given the desired size and timing constraints, the FSLOA_D_SP compiler is capable of providing suitable synchronous ROM layout instances within minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, Place & Route models, and test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold time and minimum high/low pulse widths are satisfied. This allows a more flexible clock falling edge in each operation. Only one mask of the Via1 layer is required to replace the differently coded ROM.

Logic Symbol



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