



0.15μm Standard Performance 3.3V with 5V Tolerance Generic I/Os

FSB0G_A 3.3V with 5V Tolerance Generic I/O Cells

Key Features

- UMC's 0.15μm 1.5V/3.3V Logic Standard Performance Process
- 3.3V with 5V tolerance input, 3.3V output drive
- Output buffer with programmable drive strength from 2mA to 16mA with 2mA step
- Input buffer with programmable pull up resistance, pull down resistance, keeper, and Schmitt trigger
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

This library is tailored for UMC's 0.15μm 1.5V/3.3V Logic Standard Performance Process. All I/Os are equipped with rich selections of programmable features to adapt to wide variety of application environments. Two layout structures, both optimized for pad limited and core limited designs, are available to support each programmable feature or function.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.15μm 1.5V/3.3V 1P7M SP Logic Process
	Cell Width * Cell Height	34.08μm*238.56μm (Staggered) 62.88μm*142.08μm (In-line)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M4 and above
	Layout resolution	0.005μm
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.35V to 1.65V I/O: 2.97~3.63
		Junction Temperature: -40°C ~ 125°C
	Driving Strength	2mA~16mA by 2mA step
	Input Threshold	LVTTL
	Pull Up/Down resistance	75K Ohm

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