



0.15μm Standard Performance Standard Cells - FSB0G_A Core Cell

Key Features

- UMC's 0.15μm 1.5V/3.3V Logic Standard Performance Process
- Raw gate density: 150,000 gates/mm² offers high density needed for low cost applications
- Wide drive strength range and optimized P/N ratio for performance
- Complete set of models for industry-standard EDA tools
- Support arithmetic cells for data-path designs.
- Full set of gated clock buffers for power saving
- Only Metal 1 used in layout, each cell has at least one sub / well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR drop in filler cells

General Description

This library is tailored for UMC's "0.15μm 1.5V/3.3V Logic Standard Performance Process". It is especially suitable for high speed / high density applications. The 9-track (4.32μm) cell height along with a wide selection of drive strengths enable customers to implement high performance designs with smallest area. To maximize yield, Faraday ensures all cells have no bent-gate transistors. This library can be customized to provide new cells for customers, following Faraday's internal evaluation procedures.

Quick Reference

	Characteristic	Description
Physical	Process	UMC 0.15μm 1.5V/3.3V 1P7M Logic Standard Performance Process
	Drawn Gate Length	0.15μm
	Gate Density	150,000 gates/mm ²
	Core Cell Height	4.32μm (9-track)
	Vertical / Horizontal Routing Grid	0.48μm / 0.48μm
	Power / ground rail width	0.82μm
	Layout resolution	0.005μm
Electrical	Recommended Operating Conditions	Power Supply Voltage: 1.35V to 1.65V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 29.8ps / stage (Measured from 101-stage NAND2 ring for typical process at 1.5V and 25°C)
	Power Consumption	17.68nW / MHz / gate (Measured from NAND2 chain, output load = 2 INVERTER in typical process and operated under 1.5V, 25°C)
	Drive Strengths Level	Up to 13 (Depending on cell)

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