

Key Features

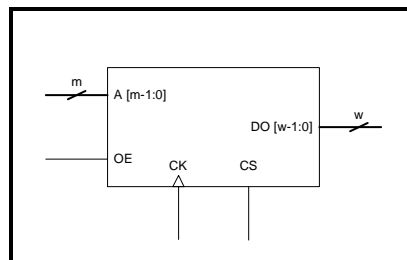
- Operating voltage range: 1.35V ~ 1.65V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 5 metal layers
- Synchronous read operation
- Fully customized layout density
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to ROM at CK rising edge
- VIA2 layer programmable codes
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout generator
- Memory compiler preview UI (Memaker)
- BIST circuitry supported
- Multi-block options for the best aspect ratio

General Description

The FSB0G_A_SC is a synchronous VIA2 Programmable ROM. It was created according to UMC's 0.15µm standard performance (SP) technology. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSB0G_A_SC compiler is capable of providing suitable synchronous ROM layout in minutes. It also automatically generates data sheets, Verilog/VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in the ASIC designs. The length of duty cycle can be neglected as long as the setup/hold time and minimum high/low pulse widths are satisfied. This allows the flexibility of clock falling edge during each operation.

Symbol



Quick Reference

Maximum Capacity	2M bits
Maximum Words	128K
Minimum Words	256
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8

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