

0.15μm Synchronous High Density Single Port SRAM Compiler – FSB0G_A_SH

Key Features

- Operating voltage range: 1.35V ~ 1.65V
- Operating junction temp. range : -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 5 metal layers
- Synchronous read and write operations
- Fully customized layout density
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to RAM with CK rising edge
- Clocked WEB input pin to RAM with CK rising edge
- Clocked DI input pins to RAM with CK rising edge
- Byte write or word write operations available
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memory compiler preview UI (Memaker)
- Column mux options for the best aspect ratio

General Description

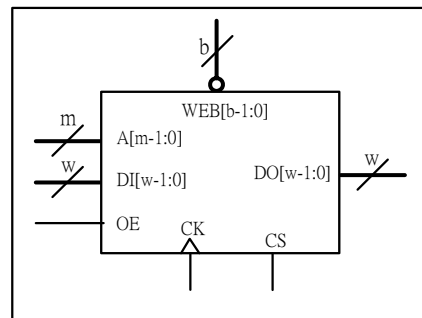
The FSB0G_A_SH is a synchronous high density, single port SRAM. It is implemented according to UMC's 0.15μm 1P7M 1.5V standard performance process design rules and can be incorporated with Faraday's 0.15μm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSB0G_A_SH compiler is capable of providing suitable synchronous RAM layout instances in minutes. It automatically generates data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This provides the flexibility of CK falling edge during each operation. Both word write and byte write operations are supported.

Quick Reference

Maximum Capacity	512k bits
Maximum Words	32K
Minimum Words	64
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux)	4, 8, 16, 32

Symbol



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