

## 0.15 $\mu$ m Standard Performance Logic Process

### FSB0G\_A\_LVPECL I/O Cells

#### Key Features

- UMC's 0.15 $\mu$ m 1.5V/3.3V Standard Performance Logic Process
- 3.3V PECL I/O cells
- Options for 25 ohms and 50 ohms output buffers
- 300MHz for differential type drivers and receivers
- 250MHz for single-ended type driver and receivers
- Support power down mode
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

#### General Description

This library is tailored for UMC's 0.15 $\mu$ m 1.5V/3.3V Standard Performance Logic Process. For high-speed chip-to-chip communications with specified DC drive characteristics, these differential type receivers and drivers provide data transfer rates up to 300Mbps. Single-ended type buffers are provided for lower power consumption. For improved noise performance (due to common mode noise rejection) these cells provide differential type buffers. Staggered and In-line structures are provided for all PECL I/O cells to fit pad limit or core limit designs.

#### Quick Reference

Characteristic		Description
<b>Physical</b>	Process	UMC 0.15 $\mu$ m 1.5V/3.3V 1P7M SP Logic Process
	Cell Width * Cell Height	34.08 $\mu$ m * 238.56 $\mu$ m (Staggered single ended input buffer)
		40.8 $\mu$ m * 238.56 $\mu$ m (Staggered single ended output buffer)
		62.88 $\mu$ m * 142.08 $\mu$ m (In-line single ended input buffer)
		69.6 $\mu$ m * 142.08 $\mu$ m (In-line single ended output buffer)
	Cell Layout Metal	M1, M2, M3
Power Ring Metal	M3 and above	
Layout Resolution	0.005 $\mu$ m	
<b>Electrical</b>	Recommended Operating Conditions	Power Supply Voltage Core: 1.35V ~ 1.65V I/O: 2.97V ~ 3.63V
		Junction Temperature: -40°C ~ 125°C
	Output Impedance	25 Ohms and 50 Ohms

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