

# Delay Locked Loop FXDLL311HB0G

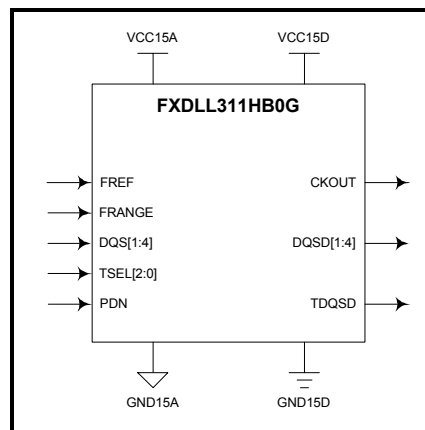
## Key Features

- UMC 0.15 $\mu$ m 1.5V standard performance process
- Operating voltage range: 1.35V ~ 1.65V
- Operating junction temperature range: -40 $^{\circ}$ C ~ 125 $^{\circ}$ C
- IP's minimum metal requirement: 4 metal layers
- Input clock frequency range: 100MHz ~ 200MHz
- DDR SDRAM controller usage
- Four channels with 20% DQS delay
- Low jitter output
- Power-down mode
- No external component required

## General Description

The FXDLL311HB0G is a 0.15 $\mu$ m Delay-Locked Loop (DLL) that generates four-channel DQS with fixed timing delay and four-channel test mode for DDR SDRAM controller usage. It can also process input clock frequencies ranging from 100MHz ~ 200MHz (DDR-200 / 266 / 333 / 400). This IP can be used in DDR SDRAM controller to generate 20% delay in period of FREF for the DQS signal to do the DQ data latch process.

## Symbol



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