

# Phase Locked Loop

## FXPLL010HB0G\_APGD

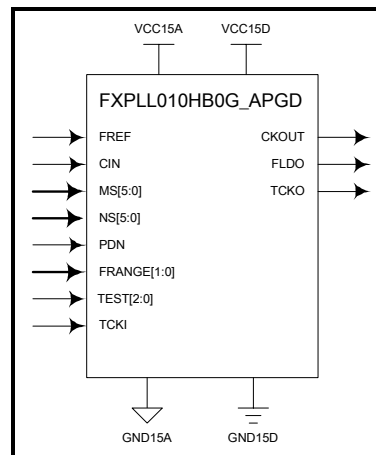
### Key Features

- UMC 0.15 $\mu$ m 1.5V Standard Process (SP)
- Operating voltage range : 1.35V~1.65V
- Operating junction temperature : -40 $^{\circ}$ C ~ 125 $^{\circ}$ C
- IP's minimum metal requirement : 3 metal layers
- Output frequency range : 20~300MHz
- 6-bit programmable pre-divider
- 6-bit programmable loop divider
- Power-down mode
- Built-in loop filter
- Built-in ESD protection circuit > 2KV (HBM)
- Built-in core limited power / ground cell

### General Description

The FXPLL010HB0G\_APGD, a 0.15 $\mu$ m Phase Locked Loop (PLL), provides a clock multiplier and/or clock de-skew circuit that can generate a stable, high-speed clock from a slower clock signal. This IP is a “generic” PLL that integrates a Voltage-Controlled Oscillator (VCO), a Phase-Frequency Detector (PFD), a Low Pass Filter (LPF), two 6-bit programmable dividers and all associated support circuitry. This IP facilitates clock multiplications from the stable crystal oscillator source. It also facilitates clock de-skews for another clock. This PLL supports an operating voltage range of 1.35V~1.65V with the operating junction temperature range of -40 $^{\circ}$ C~125 $^{\circ}$ C. This PLL can be used for DDR-200/266/333/400 application.

### Symbol



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