

3.3 V WITH 5 V TOLERANCE GENERIC I/O CELLS

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Key Features

- UMC 0.18 μm Mixmode/RFCMOS process
- Supports the 3.3 V with 5V tolerance input and 3.3 V output drives
- Supports the output buffers with the programmable drive strength from 2 mA to 8 mA in steps of 2 mA, and from 4 mA to 16 mA in steps of 4 mA
- Supports the input buffers with the enabled programmable pull-up resistance, pull-down resistance, keeper, and Schmitt-trigger features
- Built-in antenna diodes for all the pins
- ESD robustness and latch-up immunity proven by silicon

General Description

This library is tailored for UMC 0.18 μm 3.3 V with 5 V tolerance Mixmode/RFCMOS process. The I/O buffer is designed to operate at 3.3 V supply voltage. All the I/O cells are equipped with a rich selection of the programmable features capable of adapting to a wide variety of the application environments. 2 layout structures, optimized for the pad-limited and the core-limited designs respectively, are available to support each programmable feature or function.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.18 μm Mixmode/RFCOMS process
	Cell width * cell height	34.1 μm * 235.6 μm (Staggered) 62.62 μm * 140.12 μm (Inline)
	Cell layout metal	M1, M2, M3
	Power ring metal	M3, M4, M5, M6
	Layout resolution	0.01 μm
Electrical	Recommended operating conditions	Power supply voltage Core: 1.62 V ~ 1.98 V I/O: 2.97 V ~ 3.63 V Junction temperature: -40 $^{\circ}\text{C}$ ~ 125 $^{\circ}\text{C}$
	Driving strength	2 mA ~ 8 mA in steps of 2 mA 4 mA ~ 16 mA in steps of 4 mA
	Input threshold	LVTTTL
	Pull-up/Pull-down resistance	75 k Ω



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