

0.18µm Embedded High Voltage Standard Cells – FSA0V_A Core Cell

Key Features

- Raw gate density: 110,000 gates/mm², offering high density needed for low cost applications
- Complete set of models for industry-standard EDA tools
- Supports arithmetic cells for data-path designs
- Gated clock buffers for power saving
- Flexible row abutment
- Supports cells of various driving strengths
- Built-in antenna diode for all I/O cells and part of core cells
- All flip-flops have corresponding scan cells
- Rich set of AOI/AO/OAI/OA complex cells

General Description

This library, tailored for UMC's 0.18-micron 1.8 V Embedded High Voltage Process, is especially suitable for high-density applications. The 9-track (5.04-micron) cell height along with a wide selection of drive strengths enables implementation of high performance designs with smallest possible area. This library can be customized to provide new cells, following Faraday's internal evaluation procedures.

Quick Reference

	Characteristic	Description
Physical	Process	UMC 0.18-micron 1.8 V 1P6M Embedded High Voltage Process
	Drawn Gate Length	0.18 micron
	Gate Density	110,000 gates/mm ²
	Core Cell Height	5.04 micron (9-track)
	Vertical / Horizontal Routing Grid	0.56 micron / 0.62 micron
	Power / Ground Rail Width	0.76 micron
	Layout Resolution	0.01 micron
Electrical	Recommended Operating Conditions	Power Supply Voltage: 1.62 V to 1.98 V Junction Temperature: -40 °C ~ 125 °C
	Speed	Td = 47.9 ps/stage (Measured from 101-stage NAND2 ring for typical process at 1.8 V and 25 °C)
	Power Consumption	19.3 nW/MHz/gate (Measured from NAND2 chain, output load = 2 standard loads in typical process and operation under 1.8 V, 25 °C)
	Drive Strength Level	Up to 5 (depending on cell)

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