

0.18 μ m High Performance Standard Cells - FSA0A_C Core Cell

Key Features

- UMC's 0.18 μ m 1.8V GenericII Logic Process
- Raw gate density: 110,000 gates/mm² offers high density needed for low cost applications
- Wide drive strength range and optimized P/N ratio for performance
- Complete set of models for industry-standard EDA tools
- Support arithmetic cells for data-path designs
- Full set of gated clock buffers for power saving
- Only Metal 1 used in layout, each cell has at least one sub / well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR drop in filler cells

General Description

This library is tailored for UMC's 0.18 μ m 1.8V Generic II Logic Process. It is especially suitable for high speed / high density applications. The 9-track (5.04 μ m) cell height along with a wide selection of drive strengths enables customers to implement high performance designs with smallest area. This library can be customized to provide new cells for customers, following Faraday's internal evaluation procedures.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.18 μ m 1.8V/3.3V 1P6M Generic II Logic Process
	Drawn Gate Length	0.18 μ m
	Gate Density	110,000 gates/mm ²
	Core Cell Height	5.04 μ m (9-track)
	Vertical / Horizontal Routing Grid	0.56 μ m / 0.62 μ m
	Power / ground rail width	0.76 μ m
	Layout resolution	0.01 μ m
Electrical	Recommended Operating Conditions	Power Supply Voltage: 1.62V to 1.98V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 39.6ps / stage (Measured from 101-stage NAND2 ring for typical process at 1.8V and 25°C)
	Power Consumption	29nW / MHz / gate (Measured from NAND2 chain, output load = 2 INVERTER in typical process and operated under 1.8V, 25°C)
	Drive Strengths Level	Up to 8 (Depending on cell)

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