

## Key Features

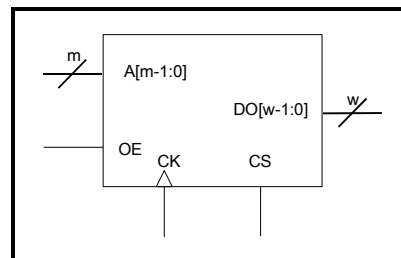
- Operating voltage range: 1.62V ~ 1.98V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 4 metal layers
- Synchronous read operation
- Fully customized layout density
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to ROM at CK rising edge
- Via-1 layer programmable codes
- Memory compiler preview UI (Memaker)
- BIST code supported
- Multi-block options for the best aspect ratio

## General Description

The FSA0A\_C\_SP is a synchronous Via1 Programmable ROM. It is implemented according to UMC's 0.18 $\mu$ m technology. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSA0A\_C\_SP compiler is capable of providing suitable synchronous ROM layout instances in minutes. It also automatically generate data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in the ASIC designs. After the setup / hold time and minimum high / low pulse width are satisfied, the duty cycle length can be neglected, which allows a flexible clock falling edge during each operation.

## Symbol



## Quick Reference

Maximum Capacity	2M bits
Maximum Words	128K
Minimum Words	256
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8

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