

0.18μm Generic II Logic Process

FSA0A_C SSTL2 (Class II) / LVTTTL (20mA) Combo I/Os

Key Features

- UMC's 0.18μm 1.8V/3.3V Generic II Logic Process
- 3.3V LVTTTL input, 3.3V LVTTTL output drive
- 2.5V SSTL2 input, 2.5V SSTL2 output drive
- Output buffer with SSTL2 (Class II) / LVTTTL (20mA) driving strength
- Input buffer with Schmitt trigger in LVTTTL mode, power down function in SSTL2 mode
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

Faraday's SSTL-2 with Class II driving strength & LVTTTL with 20mA driving strength Combo I/O cells are designed to meet JEDEC standard JESD8-9B (for SSTL-2) and JESD8-B (for LVTTTL). All SSTL-2 & LVTTTL Combo I/O cells are designed according to UMC's 0.18μm 1.8V/3.3V Generic II Logic Process.

In order to handshake with modern DDR SDRAM memory subsystem, all members in this family are designed to operate up to DDR-400 upon specified termination. By using these cells with suitable configurations, the signal convention can also be processed to provide compatibility with LVTTTL relative subsystem.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.18μm 1.8V/3.3V 1P6M Generic II Logic Process
	Cell Width * Cell Height	57.66μm * 235.6μm (Single ended bi-direction buffer)
		115.32μm * 235.6μm (Differential output buffer)
		34.1μm * 235.6μm (Single ended input buffer)
		68.2μm * 235.6μm (Differential input buffer)
	Cell Layout Metal	M1, M2, M3
Power Ring Metal	M3 and above	
Layout Resolution	0.01μm	
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.62V ~ 1.98V I/O: 2.3V~2.7V (SSTL2) I/O: 2.97V~3.63V (LVTTTL)
		Junction Temperature: -40°C ~ 125°C
		Driving Strength
	Input Threshold	SSTL2/LVTTTL

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