

0.18μm 1.8V/3.3V Generic II Logic Process FSA0A_C 3.3V Analog ESD Protection Set

Key Features

- UMC's 0.18μm 1.8V/3.3V Generic II Logic Process
- 3.3V ESD protection cells for analog I/O
- 3.3V Power / Ground cells with ESD protection
- Power-cut cells with ESD protection to separate 3.3V analog blocks from digital
- ESD robustness and Latch-up immunity proven by silicon

General Description

This I/O set is tailored for UMC's 0.18μm 1.8V/3.3V Generic II Logic Process. This set provides a full ESD protection for an isolated analog block. Two layout structures, both optimized for pad limited and core limited designs, are available.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.18μm 1.8V/3.3V 1P6M Generic II Logic Process
	Cell Height	235.6μm (Staggered) 140.12μm (In-line)
	Cell Width	Multiples of 0.62μm
	Cell Layout Metal	M1, M2
	Power Ring Metal	M3 and above
	Layout Resolution	0.01μm
Electrical	Recommended Operating Conditions	Power supply voltage Core: 1.62V to 1.98V I/O: 2.97V~3.63V
		Junction temperature: -40°C ~ 125°C

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