

0.18 μ m Generic II Logic Process

FSA0A_C PCIX 133MHz I/O Cells

Key Features

- UMC's 0.18 μ m 1.8V/3.3V Generic II Logic Process
- Support PCI33, PCI66, PCIX 133MHz
- 3.3V input, 3.3V output drive
- Input buffer with programmable pull up resistance, pull down resistance,
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

This library is tailored for UMC's 0.18 μ m 1.8V/3.3V Generic II Logic Process. All I/Os are equipped with a rich selection of programmable features capable of adapting to a wide variety of application environments. These I/O cells are designed based on "PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a" to meet PCI-X application. The PCI-X specification is specified to establish a high performance local bus standard for several generations of products.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.18 μ m 1.8V/3.3V 1P6M Generic II Logic Process
	Cell Width * Cell Height	42.78 μ m * 235.6 μ m (staggered) 62.62 μ m * 140.12 μ m (In-line)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M3 and above
	Layout resolution	0.01 μ m
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.62V to 1.98V I/O: 3.0V~3.6V
		Junction Temperature: -40°C ~ 125°C
	Driving Strength	Meet PCIX/PCI66MHz/PCI33MHz driving specification
	Input Threshold	Follow PCI Local Bus Specification
	Pull Up/Down Resistance	75K Ohm

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