

Delay Locked Loop FXDLL311HA0A

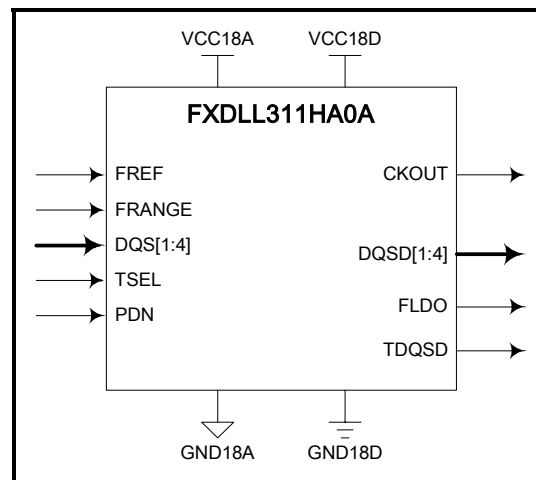
Key Features

- UMC 0.18 μ m 1.8V 1P8M Logic process
- Operating voltage range: 1.62V ~ 1.98V
- Operating junction temperature range: -40 $^{\circ}$ C ~ 125 $^{\circ}$ C
- IP's minimum metal requirement: 3 metal layers
- DDR SDRAM controller usage
- Four channels with 20% DQS delay
- Low jitter output
- Power-down mode
- No external component required
- FREF input frequency range: 100MHz~200MHz
- CKOUT output frequency range: 100MHz~200MHz

General Description

The FXDLL311HA0A is a 0.18 μ m Delay Locked Loop (DLL) IP that generates four-channel DQS with fixed timing delay and four-channel test mode for DDR SDRAM controller usage. It can also process input clock frequencies ranging from 100MHz ~ 200MHz (DDR-200 / 266 / 333 / 400). This IP can be used in DDR SDRAM controller to generate 20% DQS delay that is represented by the reference input clock (FREF) for the DQ data latch process.

Symbol



HEADQUARTERS

Hsinchu, Taiwan,
Tel: 886-3-578-7888
Fax: 886-3-578-7889
sales@faraday-tech.com.

USA OFFICE

Sunnyvale, USA
Tel: 1-408-522-8888
Fax: 1-408-522-8889
sales@faraday-usa.com

EUROPE OFFICE

Hoofddorp, Netherlands
Tel: 31-2356-20496
Fax: 31-2356-36297
eusales@faraday-tech.com

JAPAN OFFICE

Tokyo, Japan
Tel: 81-3-5214-0070
Fax: 81-3-5214-0076
sales@faraday.co.jp

CHINA OFFICE

Shanghai, P. R. China
Tel: 86-21-6406-7523
Fax: 86-21-6406-5327
sales@faraday.com.cn