

Phase Locked Loop FXPLL031HA0A_APGD

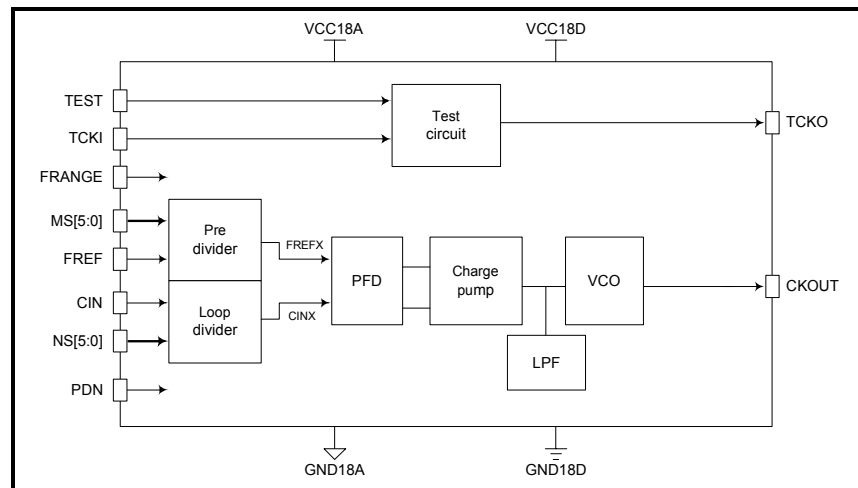
Key Features

- UMC 0.18 μ m 1.8V 1P8M Logic process
- Operating voltage range: 1.62V ~ 1.98V
- Operating junction temperature range: -40 $^{\circ}$ C ~ 125 $^{\circ}$ C
- IP's minimum metal requirement: 3 metal layers
- Power-down mode
- No external component required
- FREFX input frequency range: 5MHz~100MHz
- CKOUT output frequency range: 20MHz~300MHz
- Built-in PLL testing circuit
- Built-in ESD protection circuit
- Built-in Power/Ground pad

General Description

The FXPLL031HA0A_APGD, a 0.18 μ m Phase-Locked Loop (PLL), provides a clock multiplier and / or clock de-skew circuit that can generate a stable, high-speed clock from a slower clock signal. It is a generic PLL which integrates a Voltage-Controlled Oscillator (VCO), a Phase-Frequency Detector (PFD), a low pass filter, two 6-bit programmable dividers and all other associated supporting circuitry. This IP facilitates clock multiplications from stable crystal oscillator source. It also facilitates clock de-skews for another clock. This IP supports operating voltage range of 1.62V ~ 1.98V with the operating junction temperature in the range of -40 $^{\circ}$ C ~ 125 $^{\circ}$ C.

Block Diagram



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