



0.18μm Standard Performance Low Leakage Standard Cells – FSA0L_A Core Cell

Key Features

- UMC's 0.18μm 1.8V/3.3V 1P6M Logic Low Leakage Process
- Raw gate density: 110,000 gates/mm² offers high density needed for low cost applications
- Complete set of models for industry-standard EDA tools
- Support arithmetic cells for data-path designs
- Gated clock buffers for power saving
- Flexible row abutment
- Support cells of various driving strengths
- Build-in antenna diode for all I/O cells and parts of core cells
- All flip-flops have corresponding scan cell
- Rich set of AOI / AO / OAI / OA complex cells

General Description

This library is tailored for UMC's 0.18μm 1.8V/3.3V 1P6M low leakage logic process. It is especially suitable for low-leakage / high-density applications. The 9-track (5.04μm) cell height along with a wide selection of drive strengths enable customers to implement high performance designs with smallest area. This library can be customized to provide new cells for customers, following Faraday's internal evaluation procedures.

Quick Reference

	Characteristic	Description
Physical	Process	UMC 0.18μm 1.8V/3.3V 1P6M low leakage logic process
	Drawn Gate Length	0.18μm
	Gate Density	110,000 gates/mm ²
	Core Cell Height	5.04μm (9-track)
	Vertical / Horizontal Routing Grid	0.56μm / 0.62μm
	Power / ground rail width	0.76μm
	Layout resolution	0.01μm (0.001um for bent gate)
Electrical	Recommended Operating Conditions	Power Supply Voltage: 1.62V to 1.98V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 39.5ps/stage (Measured from 101-stage INV1 ring for typical process at 1.8V and 25°C)
	Power Consumption	29.3nW / MHz / gate (Measured from NAND2 chain, output load = 2 standard loads in typical process and operated under 1.8V, 25°C)
	Drive Strengths Level	Up to 5 (Depending on cell)

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