



0.18μm Low Leakage 3.3V with 5V Tolerance Generic I/Os FSA0L_A 3.3V with 5V Tolerance Generic I/O Cells

Key Features

- UMC's 0.18μm 1.8V/3.3V Low Leakage Logic Process
- 3.3V with 5V tolerance input, 3.3V output drive
- Output buffer with programmable drive strength from 2mA to 16mA with 2mA step
- Input buffer with programmable pull up resistance, pull down resistance, and Schmitt trigger
- Built-in Antenna diodes for all pins
- ESD Robustness and Latch-up immunity proven by Silicon

General Description

This library is tailored for UMC's 0.18μm 1.8V/3.3V Low Leakage Logic Process. All I/Os are equipped with a rich selection of programmable features capable of adapting to a wide variety of application environments. Two layout structures, both optimized for pad limited and core limited designs, are available to support each programmable feature or function.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.18μm 1.8V/3.3V 1P6M Low Leakage Logic Process
	Cell Width * Cell Height	39.68μm * 347.2μm (Staggered) 65.72μm * 225.68μm (In-line)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M3 and above
	Layout resolution	0.01μm
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 1.62V to 1.98V I/O: 2.97V~3.63V
		Junction Temperature: -40°C ~ 125°C
	Driving Strength	2mA~16mA by 2mA step
	Input Threshold	LVTTL
	Pull Up/Down resistance	75K Ohm

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