

Synchronous Low Leakage Dual-Port Static Memory Compiler – FSA0L_A_SJ

Key Features

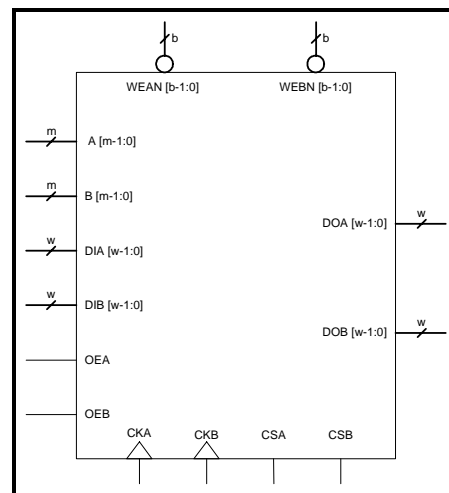
- Operating voltage range: 1.62V ~ 1.98V
- Operating junction temp. range: -40 ~ 125
- Recommended operating ambient temp. range: 0 ~ 85
- Synchronous read and write operations
- Fully customized layout density
- Minimum metal requirement: 5 metal layers
- Automatic power down to eliminate DC current
- Clocked address inputs and CSA (B) to RAM with CKA (B) rising edge
- Clocked WEA (B) N input pins to RAM with CKA (B) rising edge
- Clocked DIA (B) input pins to RAM with CKA (B) rising edge
- Byte write or word write operations available
- Verilog / VHDL timing / simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memory compiler preview UI (Memaker)
- BIST circuit supported
- Multi-block options for the best aspect ratio

General Description

The FSA0L_A_SJ is a low leakage, high density, synchronous dual-port SRAM. It is implemented according to UMC's 0.18 μ m low leakage logic process design rules. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSA0L_A_SJ compiler is capable of providing suitable synchronous SRAM layout instances in minutes. It automatically generate data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This allows the flexibility of a clock falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

Maximum Capacity	512K bits
Maximum Words	32K
Minimum Words	64
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8

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