

0.18 μ m Synchronous Low Leakage Via1 Programmable ROM Compiler – FSA0L_A_SP

Key Features

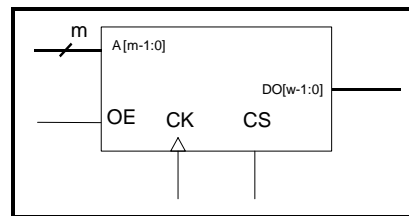
- Operating voltage range: 1.62V ~ 1.98V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 4 metal layers
- Synchronous read operations
- Fully customized layout density per customer request
- Programming using VIA1
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to ROM at CK rising edge
- Memory compiler preview UI (Memaker)
- BIST circuit supported
- Multi-block options for the best aspect ratio

General Description

The FSA0L_A_SP is a low leakage, synchronous, Via1 Programmable ROM. It is implemented according to UMC's 0.18 μ m Low Leakage Logic Process. Different combination of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSA0L_A_SP compiler is capable of providing suitable synchronous ROM layout instance in minutes. It also automatically generates data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in the ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse ranges are satisfied. This allows the flexibility of clock falling edge during each operation. Only one mask of VIA1 layer is needed to program desired coded ROM.

Symbol



Quick Reference

Maximum Capacity	2M bits
Maximum Words	128K
Minimum Words	256
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8

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