

0.18μm Synchronous Low Leakage Single Port Register File Compiler – FSA0L_A_SY

Key Features

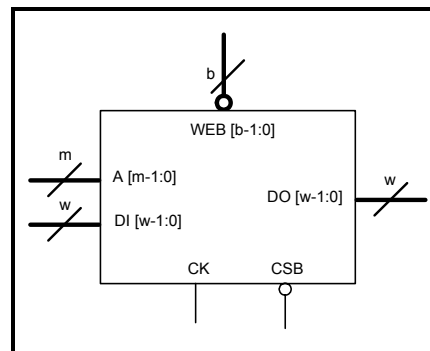
- Operating voltage range: 1.62V ~ 1.98V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 4 metal layers
- Synchronous read and write operations
- Fully customized layout density
- Automatic power down to eliminate DC current
- Clocked address inputs and CSB to RAM at CK rising edge
- Clocked WEB input pin to RAM at CK rising edge
- Clocked DI input pins to RAM at CK rising edge
- Byte write or word write operations available
- Memory compiler preview UI (Memaker)
- BIST code supported
- Column mux options for the best aspect ratio

General Description

The FSA0L_A_SY is a synchronous, single port register file. It is created according to UMC's 0.18μm 1P4M low leakage logic process design rules and can be incorporated with Faraday's 0.18μm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSA0L_A_SY compiler will provide suitable synchronous RAM layout instances in seconds. It can automatically generate data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place and route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This allows the flexibility of a clock falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

Maximum Capacity	72K bits
Maximum Words	2K
Minimum Words	8
Maximum Bits	144
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux)	2, 4, 8

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