

0.25μm High Performance Standard Cells - FS90A_C Core Cell

Key Features

- UMC's 0.25μm 2.5V Logic Process
- Raw gate density: 67,000 gates/mm² offers high density needed for low cost applications
- Wide drive strength range and optimized P/N ratio for performance
- Complete set of models for industry-standard EDA tools
- Support arithmetic cells for data-path designs
- Full set of gated clock buffers for power saving
- Each cell has at least one sub / well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR drop in filler cells

General Description

This library is tailored for UMC's 0.25μm 2.5V Logic Process. It is especially suitable for high speed / high density applications. The 8-track (6.4μm) cell height along with a wide selection of drive strengths enable customers to implement high performance designs with smallest area. This library can be customized to provide new cells for customers, following Faraday's internal evaluation procedures.

Quick Reference

Characteristic		Description
Physical	Process	UMC 0.25μm 2.5V/3.3V 1P5M Logic Process
	Drawn Gate Length	0.25μm
	Gate Density	67,000 gates/mm ²
	Core Cell Height	6.4μm (8-track)
	Vertical / Horizontal Routing Grid	0.8μm / 0.86μm
	Power / ground rail width	1.08μm
	Layout resolution	0.01μm
Electrical	Recommended Operating Conditions	Power Supply Voltage: 2.25V to 2.75V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 57.2ps / stage (Measured from 101-stage NAND2 ring for typical process at 2.5V and 25°C)
	Power Consumption	87nW / MHz / gate (Measured from NAND2 chain, output load = 2 INVERTER in typical process and operated under 2.5V, 25°C)
	Drive Strengths Level	Up to 9 (Depending on cell)

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