

Phase Locked Loop

PLL9019

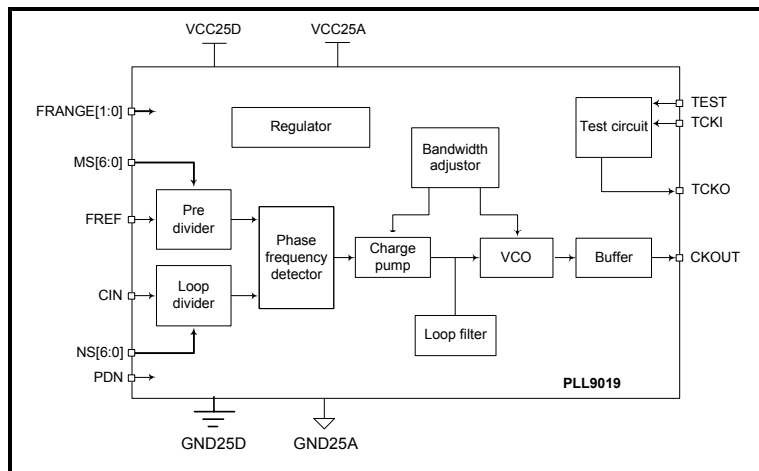
Key Features

- UMC 0.25μm 2.5V logic process
- Operating voltage range: 2.25V ~ 2.75V
- Operating junction temperature range: 0°C ~ 125°C
- IP's minimum metal requirement: 3 metal layers
- Input frequency range: 5MHz ~ 100MHz
- Output frequency range: 20MHz ~ 270 MHz
- Low jitter clock output
- 2.5V single power source
- 7-bit programmable pre-divider
- 7-bit programmable loop divider
- Built-in isolated PLL testing circuit
- Power-down mode
- Bypass mode
- Built-in loop filter

General Description

The PLL9019 is a Phase-Locked Loop (PLL) with an operating range of 20MHz ~ 270MHz. This PLL can be used in designs that are using UMC's 0.25μm, 2.5V digital CMOS process. It can be integrated on-chip to generate a high-speed clock. Having this PLL on-chip, it eliminates delays by allowing users to align the on-board clock with the on-chip clock, which de-skews the clock's distribution network. The embedded 7-bit pre-divider and loop divider allow users to boost their output frequencies up to 270MHz. This PLL works at an operating voltage range of 2.25V ~ 2.75V with operating junction temperature in the range of 0°C ~ 125°C.

Block Diagram



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