

HIGH-VOLTAGE STANDARD CELL LIBRARY

Version 1.0 | August 2008

Key Features

- 3.3 V operating voltage
- UMC 0.30 μm embedded high voltage process
- Raw gate density: 34.5k gates/ mm^2
- A wider range of drive strength and optimized P/N ratio for high performance
- A complete set of models for industry-standard EDA tools
- High density and high porosity
- 3.3 V \pm 10% characterization range
- Supports 3-corner timing models

General Description

This library is tailored for the UMC 0.30 μm embedded high voltage process. It is especially suitable for low-power, high-density applications. The 7-track (8.68 μm) cell height along with an optimized P/N ratio and a wider range of drive strengths enable the implementation of high-performance designs with a smaller area. After completing the appropriate evaluation procedures, this library can be customized to provide the cells as required.

Quick Reference

Physical	Process	UMC 0.30 μm embedded high voltage process
	Drawn gate length	0.35 μm
	Gate density	34.5k gates/ mm^2
	Core cell height	8.68 μm (7-track)
	Vertical/Horizontal routing grid	1.24 μm /1.24 μm
	Power/Ground rail width of the follow-pin routes	1.0 μm
Electrical	Recommended operating conditions	Supply voltage: 3.3 V Operating junction temperature range: -40 $^{\circ}\text{C}$ ~ 125 $^{\circ}\text{C}$
	Speed	$T_d = 105$ ps/stage, measured from the 101-stage NAND2 ring of the typical process at 3.3 V and 25 $^{\circ}\text{C}$
	Power consumption	0.16 $\mu\text{W}/\text{MHz}/\text{gate}$, measured from NAND2 chain, output load = 2 inverters in the typical process and operated at 3.3 V and 25 $^{\circ}\text{C}$
	Level of drive strength	Up to 10 levels, depending on the respective cells

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