

65 nm SYNCHRONOUS HIGH DENSITY SINGLE-PORT SRAM COMPILER WITH ROW REDUNDANCY OPTION

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Key Features

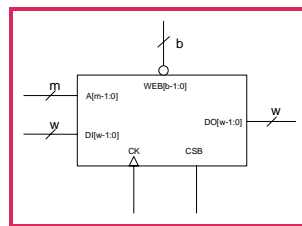
- Synchronous read and write operations
- Low leakage and AC powers
- High density available at $1.2\text{ V} \pm 10\%$
- Supports one pair of redundant row for the repair function
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs, CSB, WEB, and DI to RAM at the CK rising edge
- Supports byte write and word write operations
- Verilog/VHDL timing simulation model generator
- SPICE netlist generator
- GDSII layout generator
- Memaker preview UI
- Supports the BIST code
- Column MUX options for the best aspect ratio and speed selection

General Description

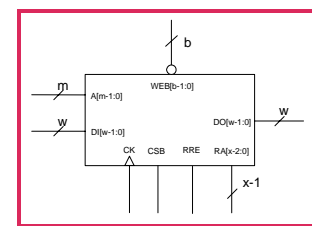
FSEOK_A_SH is a synchronous high density, single-port SRAM compiler with the row redundancy option. It is implemented by using UMC 65 nm logic LL-RVT and HVT (LowK) process design rules and can be incorporated with Faraday 65 nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configuration. There are two options available for the user to select through Memaker. (1) No redundancy (2) Row redundancy.

Given the desired size and timing constraints, the FSEOK_A_SH compiler is capable of providing the suitable synchronous RAM layout instances within minutes. It also generates the data sheets, Verilog behavioral simulation models, SCS or ViewLogic symbols, Place & Route models, and test patterns to be used in ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are satisfied. This provides a more flexible CK falling edge in each operation. Both word write and byte write operations are supported.

Symbol Diagram



Without the redundancy



With the redundancy

Quick Reference

Bit Cell	UMC 65 nm 6TSRAM0.525LLHVT
Cycle time	640 MHz (Max.) under the worse case condition for 2K x 32
Address port	One read/write port
Variable capacity	512K bits (Max.)
Aspect ratios (CM)	4, 8, 16
Application	Configurable SRAM modules for the embedded design by using UMC 65 nm logic LL-RVT and HVT (LowK) process



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