

SYNCHRONOUS SRAM COMPILER

Version 1.1 | August 2007

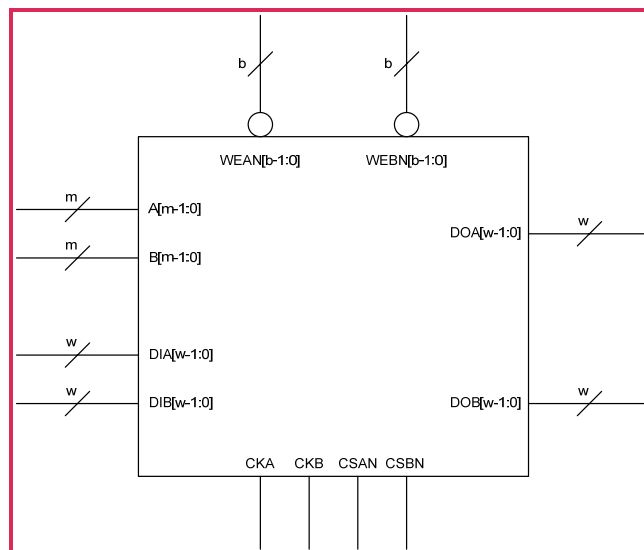
Key Features

- Synchronous read and write operations
- Low leakage device-based design
- Fully-customized layout density
- Available at $1.2\text{ V} \pm 10\%$
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CSA(B)N to the RAM at the CKA(B) rising edge
- Clocked WEA(B)N input pins to the RAM at the CKA(B) rising edge
- Clocked DIA(B) input pins to the RAM at the CKA(B) rising edge
- Supports byte write and word write operations
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST code
- Column Mux options for the best aspect ratio
- Minimum metal requirement: 6 metal layers

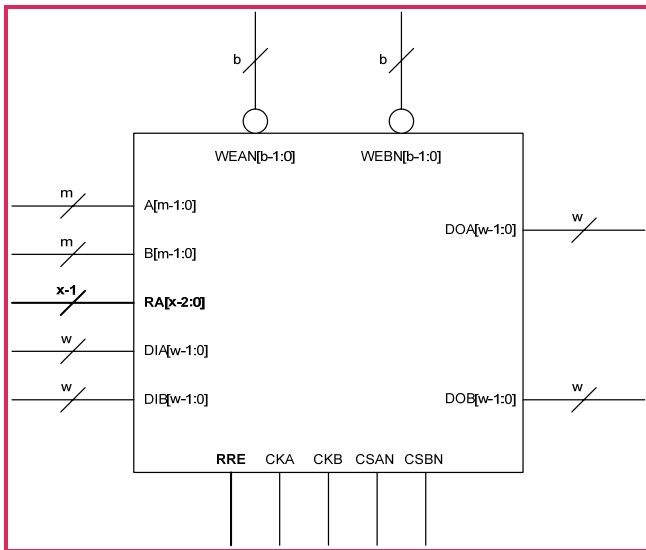
General Description

FSEOK_A_SJ is a synchronous, high density, dual-port SRAM compiler with the row redundancy option. It is implemented according to the UMC 65 nm logic LL-RVT and LL-HVT (Lowk) process design rules and can be incorporated with Faraday's 65 nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations. There are two options available for the user to select through Memaker: No redundancy or row redundancy.

Logic Symbol (Without Redundancy)



Logic Symbol (With Row Redundancy)





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