

# SYNCHRONOUS LOW-LEAKAGE VIA1 PROGRAMMABLE ROM COMPILER

Version 1.1 | August 2007

## Key Features

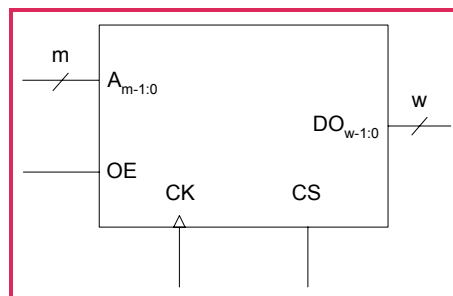
- Synchronous read operation
- Fully customized layout density per customer's configurations
- Programmable Via1 code
- High density available at 1.2 V  $\pm$ 10%
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CS to ROM at the CK rising edge
- Verilog/VHDL timing simulation model generator
- SPICE netlist generator
- GDSII layout database
- Mameker preview UI
- Supports BIST code
- Multi-block options for the best aspect ratio

## General Description

FSE0K\_A\_SP is a high density, synchronous Via1 ROM compiler. It is designed by using UMC 65 nm logic LL (LowK) process design rules and can be incorporated with Faraday 65 nm standard cells. This compiler uses different combinations of words, bits, and aspect ratios to generate the most desirable configuration.

Given the desired size and timing constraints, the FSE0K\_A\_SP compiler can provide suitable synchronous ROM layout instances within minutes. It can automatically generate the data sheets, Verilog behavioral simulation models, SCS or ViewLogic symbols, Place & Route models, and test patterns to be used in ASIC designs. The length of the duty cycle can be neglected as long as the setup and hold times and the minimum high and low pulse widths are satisfied. This provides a more flexible CK falling edge in each operation. Only one mask of the Via1 layer is required to replace for the differently coded ROM.

## Symbol Diagram



## Quick Reference

|                                   |   |
|-----------------------------------|---|
| Cycle time                        | 357 MHz (Max.) under the worst case condition of 4K x 16                                  |
| Address port                      | 1 read port   |
| Variable capacity                 | 2 MB (Max.)   |
| Output buffer                     | Tri-state   |
| Aspect ratio (Multi-block option) | 1, 2, 4, 8  |
| Application                       | Compilable ROM modules of the embedded designs by using UMC 65 nm logic LL (LowK) process |



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