

SYNCHRONOUS SINGLE-PORT REGISTER FILE SRAM COMPILER

Version 1.1 | October 2007

Key Features

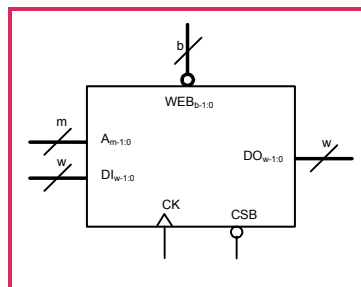
- Operating voltage range:
1.08 V ~ 1.32 V
- Operating junction temperature range:
-40 °C ~ 125 °C
- Recommended Ambient temperature
range: 0 °C ~ 85 °C
- Minimum metal requirement:
6 metal layers
- Supports synchronous read and write
operations
- Fully-customized layout density
- Available at 1.2 V \pm 10%
- Automatic power-down mechanism to
eliminate DC current
- Clocked address inputs and CSB to
RAM at the CK rising edge
- Clocked WEB input pin to RAM at the
CK rising edge
- Clocked DI input pins to RAM at the CK
rising edge
- Byte write or word write operations
available
- Verilog/VHDL timing/simulation model
generator
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- Supports the BIST code
- Column Mux options for the best aspect
ratio

General Description

FSE0K_A_SY is a synchronous, single-port register file compiler. It is implemented with UMC 65 nm logic LL-RVT and HVT (LowK) process design rules and can be incorporated with Faraday's 65 nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

Given the desired size and timing constraints, the FSE0K_A_SY compiler is capable of providing the suitable synchronous RAM layout instances in minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, SCS or ViewLogic symbols, Place & Route models, and the test patterns to be used in ASIC designs. The length of duty cycle can be neglected as long as the setup/hold time and minimum high/low pulse widths are satisfied. This provides a more flexible CK falling edge during each operation. Both word write and byte write operations are supported.

Symbol Diagram



Quick Reference

Maximum capacity	72k bits
Maximum words	2k
Minimum words	8
Maximum bits	144
Minimum bits	1
Bit increment	1
Aspect ratio (Column Mux options)	2, 4, 8



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